IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: §
GERALD DEBOY et al. §

Serial No.: **10/633,044** §

Filed: **August 1, 2003** §

Title: **"POWER FACTOR CORRECTION CIRCUIT WITH HIGH-VOLTAGE SEMICONDUCTOR COMPONENT"** §

Group Art Unit: **2815**

Examiner: **Wilson, Allan R.**

Attorney Docket No.: **068758.0134**

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37 C.F.R. §1.10

PURSUANT TO 37 CFR 1.10, I HEREBY CERTIFY THAT I HAVE KNOWLEDGE AND A REASONABLE BASIS FOR BELIEF THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS EXPRESS MAIL POST OFFICE TO ADDRESSEE ON THE DATE INDICATED BELOW, AND IS ADDRESSED TO: MAIL STOP MISSING PARTS
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INFORMATION DISCLOSURE STATEMENT

Sir:

Applicants respectfully request, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the art listed on the attached PTO-1449 forms be considered and cited in the examination of the above-identified divisional patent application.

In accordance with 37 C.F.R. §1.98(d)(1), copies of the one hundred thirty seven (137) cited art references on the attached eight (8) pages of Form PTO-1449 are not attached hereto, as each of these one hundred thirty seven (137) references was previously submitted by the Applicant, in the parent patent application U.S.S.N. 09/786,022, filed April 22, 1999, which has now been allowed and is hereby properly identified according to 37 C.F.R. §198(d)(1).

Furthermore, pursuant to 37 C.F.R. §§1.97(g) and (h), Applicants do not represent that a search has been made and do not admit that these references are, or are considered to be, material to the patentability of the present divisional application.

As this Information Disclosure Statement is being submitted before the mailing of the first office action on the merits, Applicants believe that no fee is due. However, should the Commissioner deem that a fee is due, Applicants respectfully request that the Commissioner accept this as a Petition Therefor, and authorize the Commissioner to charge any fees due to Baker Botts L.L.P. **Deposit Account No. 02-0383, Order No. 068758.0134.**

Respectfully submitted,

BAKER BOTTS L.L.P. (023640)

Date: November 4, 2003

By: _____

Andreas H. Grubert
(Limited recognition 37 C.F.R. §10.9)
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AGENT FOR APPLICANTS

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION
(Use several sheets if necessary)

Docket Number (Optional)	Application Number
068758.0102	09/786,022
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	3,171,068	02/23/65	Denkewalter et al.	317	234	10/19/60
	3,925,803	12/09/75	Kobayashi	357	22	07/12/73
	3,961,356	06/01/76	Okuhura et al.	357	50	10/31/74
	4,003,072	01/11/77	Matsushita et al.	357	52	11/01/74
	4,055,884	11/01/77	Jambotkar	29	571	12/13/76
	4,072,975	02/07/78	Ishtiani	357	23	04/22/77
	4,101,922	07/18/78	Tihanyi	357	23	03/09/77
	4,145,700	03/20/79	Jambotkar	357	23	08/08/77
	4,320,410	03/16/82	Nishizawa et al.	357	43	05/03/79
	4,345,265	08/17/82	Blanchard	357	23	04/14/80
	4,366,495	12/28/82	Goodman et al	357	23	08/06/79
	4,376,286	03/08/83	Lidow et al.	357	23	02/09/81

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation YES	NO
	EP 0 053 854 B1	16.06.82	EPO	H01L	29/06	x	
	GB 2 089 118 A	16.02.82	UK	H01L	29/78	x	
	EP 0 069 429 A2	12.01.83	EPO	H01L	29/78	x	
	EP 0 447 873 A2	01.04.92	EPO	H01L	29/784	x	
	DE 43 09 764 A1	25.03.93	Germany	H01L	29/784		x
	DE 43 09 764 C2	29.9.94	Germany	H01L	29/78		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		1967	A.S. Grove: "Physics and Technology of Semiconductor Devices" p 78-83
		1976	B. Jayant Baliga, Sorab K. Ghandi: "Analytical Solutions for the Breakdown Voltage of Abrupt Cylindrical and Spherical Junctions" (p 739-744)
		1977	Richard F. David: "Computerized Thermal Analysis of Hybrid Circuits" 27th Electronics Components Conference, May 16-18 1977 (p 324-332)

EXAMINER	DATE CONSIDERED

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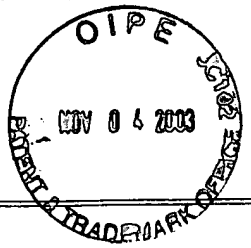

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	4,404,575	09/13/83	Nishizawa	357	22	05/03/82
	4,417,385	11/29/83	Temple	29	571	09/09/82
	4,561,003	12/24/85	Tihanyi et al.	357	23.4	04/13/84
	4,593,302	06/03/86	Lidow et al	357	23.4	08/18/80
	4,748,103	05/31/88	Hollinger	430	314	03/21/66
	4,754,310	06/28/88	Coe	357	13	12/04/84
	4,775,881	10/04/88	Ploss et al	357	30	02/13/87
	4,777,149	10/11/88	Tanabe et al.	437	142	12/22/87
	4,895,810	01/23/90	Meyers et al.	431	41	05/17/88

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation YES	Translation NO
	EP 0 772 244 A1	07.05.97	EPO	H01L	29/78	x	
	DE 196 04 043 A1	5.2.96	Germany	H01L	29/78		x
	WO 97/29518	14.08.97	PCT	H01L	29/78		x
	DE 196 04 044 A1	5.2.97	Germany	H01L	29/78		x
	WO 97/35346	25.09.97	PCT	H01L	29/78		x
	EP 0 834 926 A3	08.26.98	EPO	H01L	29/08		x
	DE 197 30 759 C1	17.7.97	Germany	H01L	29/78		x
	WO 99/04437	28.01.99	PCT	H01L	29/78		x
	WO 99/23703	14.05.99	PCT	H01L	29/06		x
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	IEEE	1977	Vinson C. Alwin, David H. Navon, Luke J. Turgeon: "Time-Dependent Carrier Flow in a Transistor Structure Under Nonisothermal Conditions" (p 1297-1304)
	IEEE	1979	Chenming Hu: "A Parametric Study of Power MOSFETS" (p 988-998)
	IEEE	1979	J.A. Appel, H.M.J. Vaes: "High Voltage Thin Layer Devices (Resurf Devices)" (p 1384-1387)

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	4,926,226	05/15/90	Heremans et al.	357	27	09/06/88
	4,941,026	07/10/90	Temple	357	23.4	08/26/88
	4,974,059	11/27/90	Kinzer	357	23.4	08/28/89
	4,975,782	12/04/90	Bauer	357	38	02/22/89
	4,994,871	02/19/91	Chang et al.	357	23.4	12/02/88
	5,008,725	04/16/91	Lidow et al.	357	23.4	12/23/88
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	5,089,434	02/18/92	Hollinser	437	41	01/22/90

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation YES	Translation NO
	WO99/36961	22.07.99	PCT	H01L	23/48		x
	DE 197 36 981C2	25.8.97	Germany	H01L	29/78		x
	EP 0 939 446 A1	01/09/99	EPO	H01L	29/08		x
	WO 00/14807	16.03.00	PCT	H01L	29/78		x
	DE 198 40 032 C1	2.9.98	Germany	H01L	29/78		x
	WO 99/62123	02.12.99	PCT	H01L	29/861		x
	DE 198 23 944 A1	28.5.98	Germany	H01L	29/861		x

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	IEEE	1979	Adrian Rusu, Contantin Bulucea: "Deep-Depletion Breakdown Voltage of Silicon-Dioxide/Silicon MOS Capacitors"v (p 201-205)
	IEEE	1979	Chenming Hu article, "Optimum Doping Profile for Minimum Ohmic Resistance and High-Breakdown Voltage"

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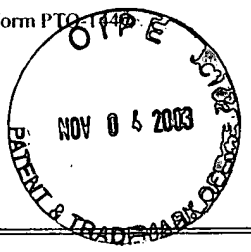

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	5,126,807	06/30/92	Baba et al.	357	23.4	06/12/91
	5,182,234	01/26/93	Meyer	437	233	07/26/91
	5,216,275	06/1/93	cHEN	257	493	09/17/91
	5,231,474	07/27/93	Hollinger	257	355	07/17/92
	5,283,201	02/01/94	Tsang et al.	437	31	08/07/92
	5,340,315	07/04/95	Rumennik	257	331	10/11/94
	5,438,215	08/01/95	Tihyani	257	401	03/25/94

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation YES	Translation NO
	WO 00/02250	13.01.00	PCT	H01L	29/10		x
	EP 0 973 203 A2	19.01.00	EPO	H01L	29/06		x
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		1979	IEDM Technical Digest excerpt (p. 239, 241)
	IEEE	1980	S.C. Sun, James D. Plummer: "Modeling of the On-Resistance of LDMOS, VDMOS, and VMOS Power Transistors" (p 356-357)
			Tihanyi and Krauss, SIPMOS, Elektronik 1980, pg. 61-64
	Springer Verlag	1980	Tihanyi , "A Qualitative Study of the DC performance of SIPMOS Transistors"
	IEEE	1980	Victor K. Temple, Robert P. Love, Peter V. Gray: "A 600-Volt MOSFET Designed for Low On-Resistance" (p 343-349)
	IEEE	1980	William A. Lane, C. Andre T. Salama: "Epitaxial VVMOS Power Transistors" (p 349-355)
	IEEE	1980	Takeaki Okabe, Isao Yoshida, Skikayuki Ochi: "A Complementary Pair of Planar-Power MOSFETS" (p 334-339)
	IEEE	1980	G. Bell, W. Ladenhauf: "SIPMOS Technology, an Example of VLSI Precision Realized with Standard LSI for Power Transistors" (p 190-194)
	UMI	December 1981	Richard A. Blanchard: "Optimization of Discrete High Power MOS Transistors"

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	5,473,180	12/05/95	Ludikhuize	257	336	07/11/94
	5,559,353	09/24/96	Risch et al.	257	334	11/01/94
	5,648,283	07/15/97	Tsang et al.	437	40	01/31/94
	5,747,831	05/05/98	Loose et al.	257	77	
	5,801,417	09/01/98	Tsang et al.	257	333	08/13/93
	5,883,411	03/16/99	Ueda et al.	257	331	11/23/92
	5,973,360	10/26/99	Tihanyi	257	330	09/21/98
	6,037,631	03/14/00	Deboy et al.	257	339	09/18/98
	US2001/0053568		Deboy et al.	438	138	03/26/01
	US2001/0050549		Deboy et al.	323	313	03/12/01

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	IEEE	1981	J.P. Stengl, H. Strack, J. Tihanyi: "Power MOS Transistors for 1000 V Blocking Voltage" (p 422-425)
	IEEE	1981	Sel Colak: "Effects of Drift Region Parameters n the same properties of Power LDMOST" (p 1455-1466)
	IEEE	1982	Min-hwa Chi, Chenming Hu: "Some Issues of Power MOSFETS" (p 392-393)
	IEEE	1982	Chen and Hu article, "Optimum Doping Profile of Power MOSFET Epitaxial Layer"
	IEEE	1983	P.L. Hower, T.M.S. Heng, C. Huang: "Optimum Design of Power MOSFETS" (p 980-984)
	IEEE	1983	Victor K. Temple: "Increased Avalanche Breakdown Voltage and Controlled Surface Electric Fields Using a Junction Termination Extension (JTE) Technique" (p 954-957)
	IEEE	1983	Victor K. Temple: "Ideal FET Doping Profile" (p 619-626)
	IEEE	1984	Board, Kenneth: "The Optimization of On-Resistance in Vertical DMOS Power Devices with Linear and Hexagonal Surface Geometries"
		June 1984	B.J. Baliga, M.S. Adler, R.P. Love et al: "Insulated Gate Transistor: A New Three-Terminal MOS-Controlled Bipolar Power Device" (excerpt) (p 1394-1402)
	IEEE	1984	Akio Nakagawa, David H. Navon: "A Time- and Temperature-Dependent 2-D Simulation of the GTO Thyristor Turn-Off Process" (p 1156-1163)

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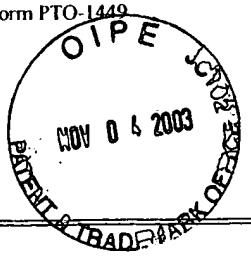

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	IEEE	1984	Chenming Hu, Min-Hwa Chi, Vikram M. Patel: "Optimum Designs of Power MOSFET's" (p 1693-1700)
	IEEE	1985	R. Stengl, U. Gösele: "Variation of Lateral Doping—A New Concept to Avoid High Voltage Breakdown of Planar Junctions" (p 154-157)
		November 1985	C. Frank Wheatley Jr., Gary M. Dolny: "COMFET—The Ultimate Power Device; A General Study of Power Devices" (p 121-128)
	Academic Press	1986	B. Jayant Baliga: "Epitaxial Silicon Technology"
			Article from Acta Electronica Sinica, March 1986, "A Novel InGaAs Phototransistor by CaO Emitter" (in Chinese) (p 35-39)
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	IEEE	1987	X.B. Chen, Z.Q. Song, Z.J. Li: "Optimization of the Drift Region of Power MOSFET's with Lateral Structures and Deep Junctions" (p 2344-2350)
	Kreiger Publishing	1987	B. Jayant Baliga: "Modern Power Devices (entire text, especially excerpt, p. 182-192, 338-339)
	IEEE	April 1987	Daisuke Ueda, Hiromitsu Takagi, Gota Kano: An Ultra-Low On-Resistance Power MOSFET Fabricated by Using a Fully Self-Aligned Process
	IEEE	1987	Wirojana Tantraporn, Victor A.K. Temple: "Multiple-Zone Single-Mask Junction Termination Extension—A High-Yield Near-Ideal Breakdown Voltage Technology" (p 220-2210)
			H.R. Chang, R.D. Black, V.A.K. Temple, Wirojana Tantraporn, B. Jayant Baliga: IEEE Transaction, November 1987; Self-Aligned UMOSFTS's with a Specific On-Resistance of 1m cm2 (p. 2329-2334)
		May 1988	Chen Xingbi, Li Zhaoji, Jiang Xu: "Two-Dimensional Numerical Analysis of High-voltage Semiconductor Electric Fields"
			Article from Chinese Journal of Semiconductors, May 1988 (p 255-260)

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	IEEE	Oct. 1988	Zahir Parpia, C. Andre T. Salama, Robert A. Hadaway, "A CMOS-Compatible High-Voltage IC Process" (p 1687-1694)
	Chinese Journal of Semiconductors	1989	Chen Xingbi, Li Zhaoji, Li Zhongmin:"Breakdown Voltage of Cylindrical Boundary Abrupt Junctions" (p 463-465)
	Solid State Electronics	1990	H.R. Chang, F.W. Holroyd: "High Voltage Power MOSFET's with a Trench-Gate Structure" (p 381-387)
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		1991	Article by Xing-Bi Chen presented at 2nd German-Chinese Electronics Week Congress, Shanghai, China.
	Chinese Journal of Semiconductors	1992	Zhang Bo, Chen Xingbi, Li Zhaoji: "Two Dimensional Electric Field Analysis of JTE Junctions" (p. 626-632)
		1998	X.B. Chen et al., "Theory of a novel voltage-sustaining layer for power devices" (from Microelectronics Journal)
			Deboy et al. article, "A New Generation of High Voltage MOSFETs breaks the Limit Line of Silicon" published by IEEE (2nd, color copy added, 2nd set of Bates ranges correspond)
		1998	Lorenz et al. article, "Drastic Reduction of On-Resistance with CoolMOS" in PCIM Europe
		May 1998	Claus Geisler, "Birth of the Cool in MOS"
		1998	X.B. Chen, P.A Mawby, K. Board et. al, "Theory of a Novel Voltage-Sustaining Layer for Power Devices" (from Microelectronics Journal)
		May 1998	Article, "Siemens Introduces new Generation of High-Voltage MOSFET Technology"
		May 1998	Article, "Siemens' new MOSFET design drastically cuts on-state resistance"
	Chinese Journal of Semiconductors	July 1998	Chen article, "Theory of a Novel Voltage Sustaining (CB) Layer for Power Devices" (from Chinese Journal of Electronics)
		July 1998	Steve Bush, "Five-fold resistance cut for high-voltage FETs"

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		1998	Lorenz et al. article, "Improved MOSFET An Important Milestone Toward a New Power MOSFET Generation" featured in PCIM
		1999	X.B. Chen et al. "High voltage sustaining structure with enbedded oppositely doped regions"
			Lai, et al.; "Characteristics and Utilization of a New Class of Low On-Resistance MOS-Gated Power Device" (1999)
		July 1999	Article "Power Semiconductors Proliferate" published in Electronics Products magazine re: Infineon CoolMOS products and IR CoolMOS- equivalent devices.
	Chinese Journal of Semiconductors	July 1999	Xing Bi Chen & Johnny K.O. Sin "A Novel High Voltage Sustaining Structure with Buried Oppositely Doped Regions"
		June 2000	Chen article, "Optimization of the Specific On-Resistance of the CoolMOS," published by IEEE Transactions on Electron Devices

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